REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-27 are pending. Claims 1-27 stand rejected.

Claims 1, 10, and 19 have been amended. Claims 9, 18, and 27 have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 103

Claims 1, 2, 4-6, 9-11, 13-15, 18-20, 22-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Publication No. 2003/0079210 of Peter Markstein et al. ("Markstein") in view of "An Experimental Study of Several Cooperative Register Allocation and Instruction Scheduling Strategies", International Symposium on Microarchitecture, Proceedings of the 28th annual international symposium on Microarchitecture, pages 169-179, 1995; by Cindy Norris and Lori L. Pollock ("Pollock"), and further in view of U.S. Patent No. 5,355,457 by Shebanow et al. ("Shebanow"). Claims 3, 12 and 21 are rejected under 35 U.S.C. 103(a) as bring unpatentable over Markstein, in view of Pollock, further in view of Shebanow, and further in view of U.S. Patent No. 5,355,457 by Todd Michael Austin ("Austin").

Applicants have amended claim 1 to indicate that modifying the program to expand a register set for a routine in the program transparently to execution of the program is performed, wherein an expanded register set is to store data used to analyze the execution of the program.

The Examiner stated Markstein does not disclose "modifying the program" and "transparently to execution of the routine" (Office Action, p.p. 3 and 4, 06/16/05).

Markstein discloses allocating registers for an intermediate language code of a program. More specifically, Markstein discloses

> In a translation and register allocation stage 101, the compiler 100 receives source code to be compiled, converts it into intermediate language and performs register allocation. During register allocation, information, such as operands from the intermediate language code, is assigned to real registers rather than intermediate registers. In an optimization stage 102, the intermediate language code is optimized, for example, using conventional optimization techniques. In a final code stage 103, the final code (e.g., machine-readable code) is generated from the intermediate code and using the previously allocated real registers.

Thus, Markstein merely discloses allocating registers to store an intermediate language code of the program in contrast to an expanded register set to store data used to analyze the execution of the program, as claimed in amended claim 1. Additionally, as set forth above, Markstein fails to disclose modifying the program transparently to execution of the program. As such, Markstein fails to disclose limitations of amended claim 1 of modifying the program to expand a register set for a routine in the program transparently to execution of the program, wherein an expanded register set is to store data used to analyze the execution of the program.

The Examiner stated that Pollock merely discloses rearranging code of a program (p. 169, " Introduction", first paragraph), and does not disclose modifying the program to expand a register set for a routine in the program transparently to execution of the program, wherein an expanded register set is to store data used to analyze the execution of the program.

Shebanow discloses logical registers, which a program manipulates during instruction execution. Each logical register is assigned a physical register from a pool of registers. More specifically, Shebanow discloses

> SEQUENCER 20 issues an instruction and the operands for that instruction are read from source logical registers, which are translated into physical registers in register files 37-39. Upon completion of the instructions, the results are written back to destination physical registers assigned to physical registers taken from the free pool. As previously indicated, source logical registers are assigned (mapped) to physical registers taken from the free pool during instruction issuance.

(Shebanow, col. 6, line 66- col. 7, line 7) (emphasis added)

Thus, Shebanow discloses assigning physical registers to store operands used by the instruction (operands for the instruction) in contrast to expanding a register set to store data used

to analyze the execution of the program, as recited in amended claim 1. As such, Shebanow fails to disclose the limitations of amended claim 1 of modifying the program to expand a register set for a routine in the program transparently to execution of the program, wherein an expanded register set is to store data used to analyze the execution of the program.

Thus, neither Markstein, Pollock, nor Shebanow discloses, teaches, or suggests such the limitations of amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103 (a) over Markstein, in view of Pollock, and further in view of Shebanow.

Given that amended independent claims 10 and 19 contain at least the discussed above limitations of amended claim 1, Applicants respectfully submit that claims 10 and 19 are likewise not obvious under 35 U.S.C. § 103 (a) over Markstein, in view of Pollock, and further in view of Shebanow.

Given that claims 2-8, 11-17, and 20-26 depend from amended independent claims 1, 10, and 19 respectively, and add additional limitations, Applicants respectfully submit that claims 2-8, 11-17, and 20-26 are likewise not obvious under 35 U.S.C. § 103 (a) over Markstein, in view of Pollock, and further in view of Shebanow.

Claims 3, 12 and 21 are rejected under 35 U.S.C. 103(a) as bring unpatentable over Markstein, in view of Pollock, further in view of Shebanow, and further in view of Austin.

Austin merely discloses registers to store pointers to program variables (col. 1, lines 29-40), and similarly to Markstein, Pollock, and Shebanow fails to disclose the limitations of amended claim 1 of modifying the program to expand a register set for a routine in the program transparently to execution of the program, wherein an expanded register set is to store data used to analyze the execution of the program.

Thus, neither Markstein, Pollock, Shebanow, nor Austin discloses, teaches, or suggests such the limitations of amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is patentable over the references cited by the Examiner.

Given that amended independent claims 10 and 19 contain at least the discussed above limitations of amended claim 1, Applicant respectfully submits that claims 10 and 19 are likewise patentable over the references cited by the Examiner.

Given that claims 2-8, 11-17, and 20-26 depend from amended independent claims 1, 10, and 19 respectively, and add additional limitations, Applicants respectfully submit that claims 2-8, 11-17, and 20-26 are likewise patentable over Markstein, in view of Pollock, further in view of Shebanow, and further in view of Austin.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome.

If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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